USE OF SOFT-DECISION OR SUM-PRODUCT INNER CODERS TO IMPROVE THE PERFORMANCE OF OUTER CODERS

RELATED APPLICATIONS

[0001] This application claims the benefit under 35 U.S.C. Section 119(e) of United States Provisional Patent Application Serial No. 60/221,851, filed on July 28, 2000, incorporated herein by reference in its entirety.

[0002] This application incorporates by reference the entire teachings of: U.S. Patent Application Ser. No. 09/846,061 entitled "Use of turbo-like codes for QAM modulation using independent I and Q decoding techniques and application to xDSL systems"; U.S. Patent Application PCT/US99/17369 entitled "Method and apparatus for design forward error correction techniques in data transmission over communications systems"; and U.S. Provisional Patent Application Ser. No. 09/702,827 entitled "Use of Turbo Trellis codes with QAM modulation for xDSL modems and other wired and wireless modems."

FIELD OF THE INVENTION

[0003] Embodiments of the invention pertain to encoder structures comprising an inner encoder, such as a Trellis Code Modulation (TCM), Turbo Code (TC) or Low Density Parity Check (LDPC) coder, and an outer encoder such as a Reed-Solomon (RS) encoder or another outer encoder. Further embodiments pertain to a corresponding decoder structure comprising an inner decoder and an outer decoder.

BACKGROUND TECHNOLOGY

[0004] Turbo codes and other receiver soft-decision extraction techniques such as Low Density Parity Check Codes (LDPC), are powerful error control techniques that allow communication at very close to the channel capacity. Low Density Parity Check Codes were introduced in 1962. The sum-product algorithm is commonly used to decode LDPC codes. The sum-product algorithm sends information forward and backward between the information bits and the parity bits iteratively, until all the bits are decoder correctly or some bits are indentified as incorrectly decoded. Consequently the sum-product algorithm provides bit error information that indicates which outputted decoded bits have errors.

[0005] LDPC encoders and decoders are conventionally used alone, and are not conventionally used in dual inner/outer coder arrangements. The efficiency of LDPC coding increases with the number of coded bits, and so conventional LDPC implementations have typically used large block sizes (e.g. one megabit) for encoding in order to achieve nearly error free operation. However, since an entire block must be received before an LDPC decoder can decode the block, the use of large blocks can introduce significant delay into the system at the receiver.

[0006] Turbo codes were introduced in 1993. Turbo-type decoders, referred to hereinafter as soft-output decoders, provide bit error probability information that indicates a probability of error for each of the decoded bits.

[0007] The use of an outer coder, such as a Reed-Solomon (RS) coder, in conjunction with an inner coder, enables errors remaining from an inner coder to be corrected by the outer coder. A RS decoder is able to correct up to R/2 errors without having information of the location of the errors. A RS decoder is able to correct up to R errors if the decoder knows where the errors are located. It is therefore desirable for an outer coder to have information indicating where errors are located. Thus the conventional outer decoder comprises two stages. The first stage receives an output bit stream from an inner decoder and determines which of the received bits have errors. The second stage uses the information generated by the first stage to selectively correct errors in the output bit stream of the inner decoder.

[0008] Examples of the use of inner and outer coders are found in the ADSL ITU recommendation G.992.1 and in the Third Mobile Generation Standard UMTS 3GPP 3G TS 25.212 V3.2.0.

[0009] The following references are incorporated by reference as representing the conventional knowledge in the field of the invention:

[0010] R. G. Gallager, "Low Density Parity-Check Codes", IRE Trans. on Information Theory, pp. 21- 28, 01/62.

[0011] C. Berrou, V. Glavieux and P. Thitimajshima, "Near Shannon limit error-correcting coding and decoding: turbo-codes", ICC 1993, Geneva, Switzerland, pp. 1064-1070, May 1993.

[0012] H. Feldman and D. V. Ramana, "An introduction to Inmarsat's New Mobile Multimedia Service", The Sixth International Mobile Satellite Conference, Ottawa, pp. 226-229, June 1999.

[0013] P. Chaudhury, W. Mohr and S. Onoe, "The 3GPP Proposal for IMT-2000", IEEE Communications Magazine, vol. 37, no 12, pp.72-81. December 1999.

[0014] 3GPP Standard "Multiplexing and channel coding: TS 25.212"

[0015] C. D. Edwards, C. T. Stelzried, L. J. Deutsch and L. Swanson, "NASAS's deep-Space Telecommunications Road Map" TMO Progress Report 42-136, JPL, Pasadena, CA USA. PP. 1-20 February 1999.

[0016] R. Pyndiah, A. Picard and A. Glavieux "Performance of Block Turbo Coded 16 QAM and 64 QAM modulations" Procedings of Globecom 95 pp.1039-1043.

[0017] Rauschmayer, Dennis J. "ADSL/VDSL Principles", Macmillan Technical Publishing, 1999.

[0018] ITU G.992.1 "ADSL Transceivers", ITU, 1999.

[0019] ITU G.992.2 "Splitterless ADSL Transceivers". ITU 1999.

[0020] ITU I.432 "B-ISDN user-network interface-physical layer specification", ITU , 1993.

[0021] Benedetto, Divsalar, Montorsi and F. Pollara, "Serial Concatenation of Interleaved Codes: Performance Analysis, Design, and Iterative Decoding", The Telecommunications and Data Acquisition Progress Report 42-126, Jet Propulsion Laboratory, Pasadena, California, pp. 1-26, August 15, 1996.

[0022] Benedetto, Divsalar, Montorsi and F. Pollara, "A Soft-Output Maximum A Posteriori (MAP) Module to decode parallel and Serial Concatenated Codes", The Telecommunications and Data Acquisition Progress Report 42-127, Jet Propulsion Laboratory, Pasadena, California, pp. 1-20, November 15, 1996.

[0023] L. R. Bahl, J. Cocke, F. Jelinek, and J. Raviv, ``Optimal Decoding of Linear Codes for Minimizing Symbol Error Rate," IEEE Transactions on Information Theory, pp. 284-287, March 1974.

[0024] Divsalar and F. Pollara, "Turbo Codes for PCS Applications", Proceedings of ICC'95, Seattle, Washington, pp. 54-59, June 1995.

[0025] D. Divsalar and F. Pollara, "Multiple Turbo Codes", Proceedings of IEEE MILCOM95, San Diego, California, November 5-8, 1995.

[0026] D. Divsalar and F. Pollara, "Soft-Output Decoding Algorithms in iterative Decoding of Turbo Codes," The Telecommunications and Data Acquisition Progress Report 42-124, Jet Propulsion Laboratory, Pasadena, California, pp. 63-87, February 15, 1995.

SUMMARY OF THE INVENTION

[0027] Embodiments in accordance with the present invention are distinguished over conventional inner/outer coder schemes in that information regarding bit errors in the output of an inner decoder is provided by the inner decoder to the outer decoder, rather than being generated internally by the outer decoder. Thus, unlike conventional outer decoders, the outer decoder in accordance with preferred embodiments of the invention does not require a conventional first stage for determining errors in the output bit stream of the inner decoder based on the bits of the output bit stream themselves.

[0028] In a first preferred embodiment, a soft-output inner decoder is utilized in a conventional manner to generate a bit stream from a received symbol stream and to generate a bit error probabilities for each bit of its output bit stream. This bit error probabilities and the output bit stream of the inner decoder are then provided to an outer decoder where errors in the output of the inner decoder are corrected in accordance with the bit error probabilities.

[0029] In a second preferred embodiment, an LDPC coder is used as an inner encoder in a transmitter, and is used as an inner decoder in a receiver. Thus, unlike in conventional implementations, the LDPC coder is employed in an inner/outer coder scheme. In a receiver, the bit error information generated by the inner LDPC decoder is provided to an outer decoder where errors in the output of the inner LDPC decoder are corrected. Because a second stage of error correction is used, it becomes possible to reduce the block size utilized for the LDPC coding.

BRIEF DESCRIPTION OF THE DRAWINGS

[0030] Figure 1 shows elements of an ADSL transmitter and receiver that use inner and outer coders;

[0031] Figure 2 shows a Coding Scheme;

[0032] Figure 3 shows a SRC Scheme;

[0033] Figure 4 shows BER curves for use of a Turbo coder as an inner encoder for the rate 4/6 64 QAM scheme in accordance with an embodiment of the invention;

[0034] Figure 5 shows BER curves for use of a Turbo coder as an inner encoder for the rate 12/14 16384 QAM scheme in accordance with an embodiment of the invention;

[0035] Figure 6 shows a process in accordance with a first preferred embodiment;

[0036] Figure 7 shows a first process in accordance with a second preferred embodiment; and

[0037] Figure 8 shows a second process in accordance with a second preferred embodiment.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

1. Introduction

[0038] The preferred embodiments of the invention presented herein pertain to encoder structures having an inner encoder comprising a soft-output coding scheme, such as Trellis Code Modulation (TCM) or Turbo Code (TC), or a Low Density Parity Check (LDPC) coding scheme. An outer encoder in accordance with the preferred embodiments comprises a Reed-Solomon (RS) encoder. However, alternative embodiments may be implemented using other inner encoders that provide bit error or bit error probability information, and using other outer encoders that utilize bit error or bit error probability information.

[0039] A first preferred embodiment exploits features of a Maximum a Posteriori (MAP) decoder used as an inner soft-output decoder. The MAP decoder provides as output a bit stream and an error probability of each bit of the bit stream (referred to herein as bit error probability information). The bit error probability information is used in the outer decoder to facilitate greater error recovery in the outer decoder (in the case of RS codes this error recovery is doubled). This scheme is contrasted with conventional implementations such as conventional xDSL modems that employ an inner decoder for TCM that uses a Viterbi decoder. This provides only hard decisions as to the value of each output bit and outputs no probability or error information that can be used in the outer RS decoder.

[0040] For purposes of comparison, the preferred embodiments of the invention will be illustrated in the context an Asymmetric Digital Subscriber Line (ADSL) system using an outer encoder and an inner encoder.

2. System model

[0041] Figure 1 shows a system model of a communication system comprising transmitting and receiving ADSL modems, such as is described in the Recommendation G.992.1 of the ITU. The system uses two dimensional multi-level signals for the inner encoder, as QAM. The transmitting modem 20 comprises a Reed-Solomon outer encoder 1, a byte interleaver 2, and an inner encoder 3 that produce an encoded bit stream from an input information bit stream. A signal-space mapper 4 maps the bit stream to symbols of a symbol constellation, and an inverse discrete Fourier transform module 5 modulates the symbols for transmission through a communication channel 6. In the receiving modem 30, a discrete Fourier transform module 7 receives the modulated signal from the communication channel 6 and converts it to a received bit stream. The receiving modem further comprises an inner decoder 8, a byte de-interleaver 9, and a Reed-Solomon outer decoder 10. The output of the outer decoder 10 is a reconstructed information bit stream.

3. Reed-Solomon (RS) encoder

[0042] The RS outer encoder 1 of Figure 1 is used very often to correct burst-errors in communication channels, such as telephone lines, deep-space communications, satellite communications, mobile communications, and CD players. The characteristic of an RS code is that it can correct up to R/2 symbols, where R is the number of check symbols used by the RS encoder.

[0043] R, the number of redundant check bytes $c_0, c_1, \ldots, c_{R-2}, c_{R-1}$ shall be appended to K information bytes $m_0, m_1, \ldots, m_{K-2}, m_{K-1}$ to form a RS codeword of size $N = K + R$ bytes. The check bytes are computed from the message byte using the equation:

$$C(D) = M(D)D^R \mod G(D) \qquad (1)$$

where:

$$M(D) = m_0 D^{K-1} + m_1 D^{K-2} + ... + m_{K-2} D + m_{K-1} \quad (2)$$

is the message polynomial,

$$C(D) = c_0 D^{R-1} + c_1 D^{R-2} + ... + c_{R-2} D + c_{R-1} \quad (3)$$

is the check polynomial, and

$$G(D) = \prod_{i=0}^{R-1} (D - \alpha^i) \quad (4)$$

is the generator polynomial of the Reed-Solomon code, where the index of the product runs from $i = 0$ to R-1. That is, C(D) is the remainder obtained from dividing M(D) D^R by G(D). The arithmetic is performed in the Galois Field GF(256), where α is a primitive element that satisfies the primitive binary polynomial $x^8 + x^4 + x^3 + x^2 + 1$ A data byte (d_7, d_6, ... , d_1, d_0) is identified with the Galois Field element $d_7\alpha^7 + d_6\,\alpha^6 + ... + d_1\,\alpha + d_0$

[0044] With this definition RS is able to correct up to R/2 symbols. If there are more than R/2 symbols with errors, RS will not be able to correct any of them. Because of this characteristic of RS, a high value for R is used, to make sure that the system is working error-free (assuming impulse noise of duration inferior to 0.5 ms).

[0045] The values of the redundancy to work error free are around 10-15%.

[0046] To improve the performance of the RS outer encoder, a byte interleaver 2 is used as indicated in Figure 1.

3. The soft-inner encoder-decoder

[0047] In accordance with the first preferred embodiment, the inner encoder 3 of Figure 1 is a TC. Two examples are provided herein addressing the cases of 64 QAM and 16384 QAM modulations to show how information about the probability of each symbol can be use to improve the performance of a RS outer encoder. The signal-space mapper 4 of Figure 1 in these cases provides independent I&Q QAM Gray mapping.

3.1. Description of the method for implementation

3.1.1 Capacity Bounds

[0048] The minimum E_b/N_0 values to achieve the Shannon bound 64 QAM and 16384 QAM bounds for spectral efficiencies of 4 and 12 bits/s/Hz respectively are as in Table 1 for a BER=10^{-5}.

Table 1. Shannon bounds.

Spectral efficiency η [bit/s/Hz]	Shannon bound Eb/No [dB]
4	5.6
12	24.7

[0049] The conversion from SNR of the QAM signal to E_b / N_0 is performed using the following relation:

$$E_b / N_0[dB] = SNR\ [dB] - 10\ log_{10}(\eta)\ [dB] \quad (5)$$

where η is the number of information bits per symbol.

[0050] For a D-dimension modulation the following formulae are used:

$$SNR = \frac{E[|a_k^2|]}{E[|w_k^2|]} = \frac{E[|a_k^2|]}{D\sigma_N^2} = \frac{E_{av}}{D\sigma_N^2} \quad (6)$$

$$SNR = \frac{E_s}{D\frac{N_0}{2}} = \frac{\eta E_b}{D\frac{N_0}{2}} \quad (7)$$

where σ^2_N is the noise variance in each of the D dimension and η is the number of information bits per symbol. From the above relations:

$$\sigma_N^2 = E_{av}\left(\frac{2\eta E_b}{N_0}\right)^{-1} \quad (8)$$

3.1.2 Coding

[0051] The coding scheme is shown in Figure 2. The two systematic recursive codes (SRC) used are identical and are defined in Figure 3. The code is described by the generating polynomials 35o and 23o.

3.1.3 Turbo code internal interleaver.

[0052] The interleaver of this embodiment is an LRI interleaver. The interleaving sequence of the LRI is as follows:

[0053] Determination of the interleaving buffer size.

M: Number of column in the interleaving buffer (M > 16).

N: Number of rows in the interleaving buffer (N > 16).

BL: Interleaving block size (BL= PxP >= MxN).

P: Minimum prime number that is larger than M.

v: Minimum primitive root of P.

[0054] Making basic random set whose length is M

$$C(0) = 1 ; \quad C(i+1) = v \times C(i) \bmod P, \qquad i = 0,1,....P-3 \tag{9}$$

[0055] Making j-th inter-row permutation pattern.

By shifting output of step 2 one by one per inter-row, a Latin square matrix is made. The last (M-1)th column is processed specially in order to avoid low hamming weight phenomenon caused by the forced termination.

$$CLj\,(i) = C\,(j + i \bmod M-1) \; ; \quad CLj(M-1) = 0 \; ; \; i = 0,1,...M-2 \; ; \quad j = 0,1,...,N-1 \tag{10}$$

[0056] Row by row 2D-mapping of di to MxN buffer.

$$d^*j\,(i) = i+Mxj \; , \; i = 0,1,...,M-2 \; ; \; j=0,1,...,N-1 \tag{11}$$

[0057] Permutating of 2D-mapped input set di by the permutation pattern made in point 3.

$$d^{**}j(i) = d^*\,(N-j)\,(CL)N-j)\,(i)), \; , \; i = 0,1,...,M-1; j = 0,1,...,N-1 \tag{12}$$

[0058] Reading a permuted input set column by column, and making output set.

$$d'(j+Nxi) = d^{**}j(i) \; , \; i = 0,1,...,M-1; j = 0,1,...,N-1 \tag{13}$$

[0059] Pruning bits.

d' is pruned by deleting the l-bits in order to adjust the output d' to the input block length BL, where the deleted bits are non-existent bits in the input sequence. The pruning number L is defined as L = MxN - BL.

3.1.4. Coding And Modulation For 4 Bit/S/Hz Spectral Efficiency.

3.1.4.1 Puncturing

[0060] In order to obtain a rate 4/6 code, the puncturing pattern used is shown in Table 2.

Table 2. Puncturing and Mapping for Rate 4/6 64 QAM

Information bit (d)	d_1	d_2	d_3	d_4
parity bit (p)	p_1	-	-	-
parity bit (q)	-	-	q_3	-
8AM symbol (I)	(d_1, d_2, p_1)			
8AM symbol (Q)	(d_3, d_4, q_3)			
64 QAM symbol (I , Q)	$(I, Q)=(d_1, d_2, p_1, d_3, d_4, q_3)$			

3.1.4.2 Modulation

[0061] In this embodiment Gray mapping is used in each dimension. Four information bits are required to be sent using a 64 QAM constellation. For a rate 4/6 code and 64 QAM, the noise variance in each dimension is

$$E_{av} = (8(49+25+9+1+25+49+49+9+49+1+25+9+25+1+9+1))\,A^2/64 = 42\,A^2 \quad (14)$$

$$\sigma_N^2 = E_{av}\left(\frac{2\eta E_b}{N_0}\right)^{-1} = 42\,A^2\left(\frac{2 \times 4 \times E_b}{N_0}\right)^{-1} = 5.25\,A^2\left(\frac{E_b}{N_0}\right)^{-1} \quad (15)$$

[0062] The puncturing and mapping scheme is shown in Table 2 for 4 consecutive information bits that are encoded into 6 coded bits, therefore one 64 QAM symbol. The turbo encoder with the puncturing presented in Table 2 is a rate 4/6 turbo code which in conjunction with 64 QAM gives a spectral efficiency of 4 bits/s/Hz. Considering two independent Gaussian noises with identical variance σ^2_N, the LLR can be determined independently for each I and Q. It is assumed that at time k u_1^k, u_2^k and u_3^k modulate the I

component and u_4^k, u_5^k and u_6^k modulate the Q component of the 64 QAM scheme. At the receiver, the I and Q signals are treated independently in order to take advantage of the simpler formulae for the LLR values.

3.1.4.3 Bit Probabilities

[0063] From each received symbol, the bit probabilities for the three I dimension bits are computed as follows:

$$LLR(u_1^k) = \log\left(\frac{\sum_{i=1}^{4}\exp[-\frac{1}{2\sigma_N^2}(I^k - a_{1,i}^k)^2]}{\sum_{i=1}^{4}\exp[-\frac{1}{2\sigma_N^2}(I^k - a_{0,i}^k)^2]}\right) = \tag{16}$$

$$= \log\left(\frac{\exp[-\frac{1}{2\sigma_N^2}(I^k - A_4)^2] + \exp[-\frac{1}{2\sigma_N^2}(I^k - A_5)^2] + \exp[-\frac{1}{2\sigma_N^2}(I^k - A_6)^2] + \exp[-\frac{1}{2\sigma_n^2}(I^k - A_7)^2]}{\exp[-\frac{1}{2\sigma_N^2}(I^k - A_0)^2] + \exp[-\frac{1}{2\sigma_N^2}(I^k - A_1)^2] + \exp[-\frac{1}{2\sigma_N^2}(I^k - A_2)^2 + \exp[\frac{1}{2\sigma_N^2}(I^k - A_3)^2]}\right)$$

$$LLR(u_2^k) = \log\left(\frac{\sum_{i=1}^{4}\exp[-\frac{1}{2\sigma_N^2}(I^k - a_{1,i}^k)^2]}{\sum_{i=1}^{4}\exp[-\frac{1}{2\sigma_N^2}(I^k - a_{0,i}^k)^2]}\right) = \tag{17}$$

$$= \log\left(\frac{\exp[-\frac{1}{2\sigma_N^2}(I^k - A_2)^2] + \exp[-\frac{1}{2\sigma_N^2}(I^k - A_3)^2] + \exp[-\frac{1}{2\sigma_N^2}(I^k - A_6)^2] + \exp[-\frac{1}{2\sigma_n^2}(I^k - A_7)^2]}{\exp[-\frac{1}{2\sigma_N^2}(I^k - A_0)^2] + \exp[-\frac{1}{2\sigma_N^2}(I^k - A_1)^2] + \exp[-\frac{1}{2\sigma_N^2}(I^k - A_4)^2 + \exp[\frac{1}{2\sigma_N^2}(I^k - A_5)^2]}\right)$$

$$LLR(u_3^k) = \log\left(\frac{\sum_{i=1}^{4}\exp[-\frac{1}{2\sigma_N^2}(I^k - a_{1,i}^k)^2]}{\sum_{i=1}^{4}\exp[-\frac{1}{2\sigma_N^2}(I^k - a_{0,i}^k)^2]}\right) = \tag{18}$$

$$= \log\left(\frac{\exp[-\frac{1}{2\sigma_N^2}(I^k - A_1)^2] + \exp[-\frac{1}{2\sigma_N^2}(I^k - A_5)^2] + \exp[-\frac{1}{2\sigma_N^2}(I^k - A_3)^2] + \exp[-\frac{1}{2\sigma_n^2}(I^k - A_7)^2]}{\exp[-\frac{1}{2\sigma_N^2}(I^k - A_0)^2] + \exp[-\frac{1}{2\sigma_N^2}(I^k - A_4)^2] + \exp[-\frac{1}{2\sigma_N^2}(I^k - A_2)^2 + \exp[\frac{1}{2\sigma_N^2}(I^k - A_6)^2]}\right)$$

[0064] An analogous computation effort is required for the bits of the Q dimension, the I^k being replaced with the Q^k demodulated value in order to evaluate LLR(u_4^k), LLR(u_5^k) and LLR(u_6^k).

[0065] The bit error probabilities are provided to the outer decoder where they are used by the outer decoder to detect the location of the erroneous bits and to selectively correct the erroneous bits.

[0066] As discussed above, conventional outer decoders comprise a first stage that determines bit error information from the output bits of the inner decoder themselves, and a second stage that corrects bits in accordance with the bit error information. In accordance with the first preferred embodiment of the present invention, the first stage of the conventional outer decoder is replaced with a stage that generates a hard bit error decision for each bit using externally provided bit error probability information, such as by a thresholding procedure, and provides the bit error information to a second stage, such a conventional second stage, where bit errors are corrected in accordance with the bit error information. Those of ordinary skill in the art will be capable of modifying any of the conventional outer decoders of this type to accept externally generated bit error probability information and generated bit error information therefrom for use in the second stage of the decoder. Therefore no further detailed discussion of the outer decoder is provided here apart from the discussion in section 5 below.

3.1.4.4 Simulation Results

[0067] Figure 4 shows simulation results for 10,400 information bits with an S-type interleaver. A BER of 10^{-7} can be achieved after 8 iterations at $E_b/N_0 = 8.3$ dB.

3.1.5 Coding And Modulation For 12 Bit/S/Hz Spectral Efficiency.

[0068] A second example in accordance with the first preferred embodiment utilizes a rate 12/14 coding scheme with 16384 QAM.

3.1.5.1 Puncturing

[0069] In order to obtain a rate 12/14 code, a puncturing pattern as shown in Table 3 is used.

Table 3. Puncturing and Mapping for Rate 12/14 16384 QAM

Information bit (d)	d_1	d_2	d_3	d_4	d_5	d_6	d_7	d_8	d_9	d_{10}	d_{11}	d_{12}
parity bit (p)	p_1											
parity bit (q)							q_7					
128AM symbol (I)	$(d_1, d_2, d_3, d_4 d_5, d_6, p_1)$											
128AM symbol (Q)	$(d_7, d_8, d_9, d_{10}, d_{11}, d_{12}, p_7)$											
16384 QAM symbol (I , Q)	$(d_1, d_2, d_3, d_4 d_5, d_6, p_1, d_7, d_8, d_9, d_{10}, d_{11}, d_{12}, p_7)$											

3.1.5.2 Modulation

[0070] For a 16384 QAM constellation with points at –127A, -125A, -123A, -121A, -119A, -117A, -115A, -113A, -111A, -109A, -107A, -105A, -103A, -101A, -99A, -97A, -95A, -93A, -91A, -89A, -87A, -85A, -83A, -81A, -79A, -77A, -75A, -73A, -71A, -69A, -67A, -65A, -63A, -61A, -59A, -57A, -55A, -53A, -51A, -49A, -47A, -45A, -43A, -41A, -39A, -37A, -35A, -33A, -31A, -29A, -27A, -25A, -23A, -21A, -19A, -17A, –15A, -13A, -11A, -9A, -7A, -5A, -3A, -A, A, 3A, 5A, 7A, 9A, 11A, 13A, 15A, 17A, 19A, 21A, 23A, 25A, 27A, 29A, 31A, 33A, 35A, 37A, 39A, 41A, 43A, 45A, 47A, 49A, 51A, 53A, 55A, 57A, 59A, 61A, 63A, 65A, 67A, 69A, 71A, 73A, 75A, 77A, 79A, 81A, 83A, 95A, 87A, 89A, 91A, 93A, 95A, 97A, 99A, 101A, 103A, 105A, 107A, 109A, 111A, 113A, 115A, 117A, 119A, 121A, 123A, 125A, 127A, E_{av} is:

$$E_{av} = 5461\ A^2 \tag{19}$$

[0071] It is assumed that at time k the symbol $u^k = (u_1^k, u_2^k, u_3^k, u_4^k, u_5^k, u_6^k, u_7^k, u_8^k, u_9^k, u_{10}^k, u_{11}^k, u_{12}^k, u_{13}^k, u_{14}^k)$ is sent though the channel. It is assumed that at time k the symbol $u_1^k, u_2^k, u_3^k, u_4^k, u_5^k, u_6^k$ and u_7^k modulate the I component and $u_8^k, u_9^k, u_{10}^k\ u_{11}^k, u_{12}^k, u_{13}^k$ and u_{14}^k modulate the Q component of a 16384 QAM scheme.

[0072] For a rate 12/14 code and 16384 QAM, the noise variance is:

$$\sigma_N^2 = E_{av}\left(\frac{2\eta E_b}{N_0}\right)^{-1} = 5461\,A^2\left(\frac{2 \times 6 \times E_b}{N_0}\right)^{-1} = 455.08\,A^2\left(\frac{E_b}{N_0}\right)^{-1} \tag{20}$$

[0073] In order to study the performance of this scheme, a rate 6/7 turbo code and a 128AM is used. The 16384 QAM scheme will achieve a similar performance in terms of bit

error rate (BER) at twice the spectral efficiency, assuming an ideal demodulator. The puncturing and mapping scheme shown in Table 8 is for 12 consecutive information bits that are coded into 14 encoded bits, therefore, one 16384 QAM symbol. The turbo encoder is a rate 12/14 turbo code, which in conjunction with 16384 QAM, gives a spectral efficiency of 12 bits/s/Hz.

3.1.5.3 Bit Probabilities

[0074] The 128AM symbol is defined as $u^k = (u_1^k, u_2^k, u_3^k, u_4^k, u_5^k, u_6^k, u_7^k)$, where u_1^k is the most significant bit and u_7^k is the least significant bit . The following set can be defined.

[0075] bit-1-is-0 = $\{A_0, A_1, A_2, A_3, A_4, A_5, A_6, A_7, A_8, A_9, A_{10}, A_{11}, A_{12}, A_{13}, A_{14}, A_{15}, A_{16}, A_{17}, A_{18}, A_{19}, A_{20}, A_{21}, A_{22}, A_{23}, A_{24}, A_{25}, A_{26}, A_{27}, A_{28}, A_{29}, A_{30}, A_{31}, A_{32}, A_{33}, A_{34}, A_{35}, A_{36}, A_{37}, A_{38}, A_{39}, A_{40}, A_{41}, A_{42}, A_{43}, A_{44}, A_{45}, A_{46}, A_{47}, A_{48}, A_{49}, A_{50}, A_{51}, A_{52}, A_{53}, A_{54}, A_{55}, A_{56}, A_{57}, A_{58}, A_{59}, A_{60}, A_{61}, A_{62}, A_{63}\}$

[0076] bit-1-is-1 = $\{A_{64}, A_{65}, A_{66}, A_{67}, A_{68}, A_{69}, A_{70}, A_{71}, A_{72}, A_{73}, A_{74}, A_{75}, A_{76}, A_{77}, A_{78}, A_{79}, A_{80}, A_{81}, A_{82}, A_{83}, A_{84}, A_{85}, A_{86}, A_{87}, A_{88}, A_{89}, A_{90}, A_{91}, A_{92}, A_{93}, A_{94}, A_{95}, A_{96}, A_{97}, A_{98}, A_{99}, A_{100}, A_{101}, A_{102}, A_{103}, A_{104}, A_{105}, A_{106}, A_{107}, A_{108}, A_{109}, A_{110}, A_{111}, A_{112}, A_{113}, A_{114}, A_{115}, A_{116}, A_{117}, A_{118}, A_{119}, A_{120}, A_{121}, A_{122}, A_{123}, A_{124}, A_{125}, A_{126}, A_{127}\}$

[0077] bit-2-is-0 = $\{A_0, A_1, A_2, A_3, A_4, A_5, A_6, A_7, A_8, A_9, A_{10}, A_{11}, A_{12}, A_{13}, A_{14}, A_{15}, A_{16}, A_{17}, A_{18}, A_{19}, A_{20}, A_{21}, A_{22}, A_{23}, A_{24}, A_{25}, A_{26}, A_{27}, A_{28}, A_{29}, A_{30}, A_{31}, A_{96}, A_{97}, A_{98}, A_{99}, A_{100}, A_{101}, A_{102}, A_{103}, A_{104}, A_{105}, A_{106}, A_{107}, A_{108}, A_{109}, A_{110}, A_{111}, A_{112}, A_{113}, A_{114}, A_{115}, A_{116}, A_{117}, A_{118}, A_{119}, A_{120}, A_{121}, A_{122}, A_{123}, A_{124}, A_{125}, A_{126}, A_{127}\}$

[0078] bit-2-is-1 = $\{A_{32}, A_{33}, A_{34}, A_{35}, A_{36}, A_{37}, A_{38}, A_{39}, A_{40}, A_{41}, A_{42}, A_{43}, A_{44}, A_{45}, A_{46}, A_{47}, A_{48}, A_{49}, A_{50}, A_{51}, A_{52}, A_{53}, A_{54}, A_{55}, A_{56}, A_{57}, A_{58}, A_{59}, A_{60}, A_{61}, A_{62}, A_{63}, A_{64}, A_{65}, A_{66}, A_{67}, A_{68}, A_{69}, A_{70}, A_{71}, A_{72}, A_{73}, A_{74}, A_{75}, A_{76}, A_{77}, A_{78}, A_{79}, A_{80}, A_{81}, A_{82}, A_{83}, A_{84}, A_{85}, A_{86}, A_{87}, A_{88}, A_{89}, A_{90}, A_{91}, A_{92}, A_{93}, A_{94}, A_{95}\}$

[0079] bit-3-is-0 = {A_0 ,A_1 , A_2 , A_3 , A_4 , A_5 , A_6 , A_7 , A_8 ,A_9 , A_{10} , A_{11} , A_{12} , A_{13} , A_{14} , A_{15}, A_{48}, A_{49}, A_{50} , A_{51} , A_{52} , A_{53} , A_{54} , A_{55} , A_{56} ,A_{57} , A_{58} , A_{59} , A_{60} , A_{61} , A_{62} , A_{63}, A_{64}, A_{65}, A_{66}, A_{67}, A_{68}, A_{69}, A_{70}, A_{71}, A_{72}, A_{73}, A_{74}, A_{75}, A_{76}, A_{77}, A_{78}, A_{79}, A_{112}, A_{113}, A_{114}, A_{115}, A_{116}, A_{117}, A_{118}, A_{119}, A_{120}, A_{121}, A_{122}, A_{123}, A_{124}, A_{125}, A_{126} , A_{127}}

[0080] bit-3-is-1 = {A_{16} ,A_{17} , A_{18} , A_{19}, A_{20} , A_{21} , A_{22} , A_{23} , A_{24} ,A_{25} , A_{26} , A_{27} , A_{28} , A_{29} , A_{30} , A_{31}, A_{32} ,A_{33} , A_{34} , A_{35} , A_{36} , A_{37} , A_{38} , A_{39} , A_{40} ,A_{41} , A_{42} , A_{43} , A_{44} , A_{45} , A_{46} , A_{47}, A_{80}, A_{81} , A_{82} , A_{83}, A_{84} , A_{85} , A_{86} , A_{87} , A_{88} ,A_{89} , A_{90} , A_{91} , A_{92} , A_{93} , A_{94} , A_{95} , A_{96}, A_{97} , A_{98} , A_{99} , A_{100}, A_{101}, A_{102}, A_{103}, A_{104}, A_{105}, A_{106}, A_{107}, A_{108}, A_{109}, A_{110} , A_{111} }

[0081] bit-4-is-0 = {A_0 ,A_1 , A_2 , A_3 , A_4 , A_5 , A_6 , A_7 , A_{24} ,A_{25} , A_{26} , A_{27} , A_{28} , A_{29} , A_{30} , A_{31} A_{32} ,A_{33} , A_{34} , A_{35} , A_{36} , A_{37} , A_{38} , A_{39} , A_{56} ,A_{57} , A_{58} , A_{59} , A_{60} , A_{61} , A_{62} , A_{63}, A_{64}, A_{65}, A_{66} , A_{67} , A_{68} , A_{69} , A_{70} , A_{71} ,A_{88} ,A_{89} , A_{90} , A_{91} , A_{92} , A_{93} , A_{94} , A_{95} , A_{96} ,A_{97} , A_{98} , A_{99} , A_{100}, A_{101}, A_{102}, A_{103}, A_{120}, A_{121}, A_{122}, A_{123}, A_{124}, A_{125} , A_{126} , A_{127} }

[0082] bit-4-is-1 = {A_8 ,A_9 , A_{10} , A_{11} , A_{12} , A_{13} , A_{14} , A_{15} , A_{16} ,A_{17} , A_{18} , A_{19}, A_{20} , A_{21} , A_{22} , A_{23} , A_{40} ,A_{41} , A_{42} , A_{43} , A_{44} , A_{45} , A_{46} , A_{47} ,A_{48}, A_{49} , A_{50} , A_{51} , A_{52} , A_{53} , A_{54} , A_{55} , A_{72} ,A_{73} , A_{74} , A_{75} , A_{76} , A_{77} , A_{78} , A_{79} ,A_{80} ,A_{81} , A_{82} , A_{83}, A_{84} , A_{85} , A_{86} , A_{87} , A_{104}, A_{105}, A_{106}, A_{107}, A_{108}, A_{109}, A_{110} , A_{111}, A_{112}, A_{113}, A_{114}, A_{115}, A_{116}, A_{117}, A_{118}, A_{119}, }

[0083] bit-5-is-0 = {A_0 ,A_1 , A_2 , A_3 , , A_{12} , A_{13} , A_{14} , A_{15} , A_{16} ,A_{17} , A_{18} , A_{19}, , A_{28} , A_{29} , A_{30}, A_{31} , A_{32} ,A_{33} , A_{34} , A_{35} , A_{44} , A_{45} , A_{46} , A_{47}, A_{48}, A_{49} , A_{50} , A_{51} , , A_{60} , A_{61} , A_{62} , A_{63} A_{64}, A_{65}, A_{66} , A_{67}, A_{76} , A_{77} , A_{78} , A_{79} , A_{80} ,A_{81} , A_{82} , A_{83}, A_{92} , A_{93} , A_{94} , A_{95} , A_{96} , A_{97}, A_{98} , A_{99}, A_{108}, A_{109}, A_{110}, A_{111} ,A_{112}, A_{113}, A_{114}, A_{115}, A_{124}, A_{125} , A_{126} , A_{127}}

[0084] bit-5-is-1 = {A_4 , A_5 , A_6 , A_7 , A_8 ,A_9 , A_{10} , A_{11}, A_{20} , A_{21} , A_{22} , A_{23} , A_{24} ,A_{25} , A_{26} , A_{27} A_{36} , A_{37} , A_{38} , A_{39} , A_{40} ,A_{41} , A_{42} , A_{43} , A_{52} , A_{53} , A_{54} , A_{55} , A_{56} ,A_{57} , A_{58} , A_{59} , A_{68} , A_{69} , A_{70} , A_{71} , A_{72} ,A_{73} , A_{74} , A_{75}, A_{84} , A_{85} , A_{86} , A_{87} , A_{88} ,A_{89} , A_{90} , A_{91}, A_{100}, A_{101}, A_{102}, A_{103}, A_{104} ,A_{105}, A_{106}, A_{107}, A_{116}, A_{117}, A_{118}, A_{119}, A_{120}, A_{121}, A_{122}, A_{123}}

[0085] bit-6-is-0 = {A_2 , A_3 , A_4 , A_5 , A_{10} , A_{11} , A_{12} , A_{13}, A_{18} , A_{19}, A_{20} , A_{21} , A_{26} , A_{27} , A_{28} , A_{29}, A_{34} , A_{35} , A_{36} , A_{37} , A_{42} , A_{43} , A_{44} , A_{45} , A_{50} , A_{51} , A_{52} , A_{53} ,A_{58} , A_{59}, A_{60}, A_{61} , A_{66} , A_{67}, A_{68} , A_{69} A_{74} , A_{75} , A_{76} , A_{77} A_{82} , A_{83}, A_{84} , A_{85} , A_{90} , A_{91} , A_{92} , A_{93} , A_{98} , A_{99} , A_{100}, A_{101} A_{106}, A_{107}, A_{108}, A_{109} A_{114}, A_{115}, A_{116}, A_{117} A_{122}, A_{123}, A_{124}, A_{125}}

[0086] bit-6-is-1 = {A_0 ,A_1 A_6 , A_7 , A_8 ,A_9, A_{14} , A_{15}, A_{16} ,A_{17} A_{22} , A_{23} , A_{24} ,A_{25}, A_{30} , A_{31} , A_{32} ,A_{33} A_{38} , A_{39} , A_{40} ,A_{41} A_{46} , A_{47}, A_{48}, A_{49} A_{54} , A_{55} , A_{56} ,A_{57} A_{62} , A_{63}, A_{64}, A_{65}, A_{70} , A_{71} , A_{72} ,A_{73} , A_{78} , A_{79}, A_{80} ,A_{81} , A_{86} , A_{87} , A_{88} ,A_{89} , A_{94} , A_{95} A_{96} ,A_{97}, A_{102}, A_{103}, A_{104} , A_{105}, A_{110} , A_{111} , A_{112}, A_{113}, A_{118}, A_{119}, A_{120}, A_{121}, A_{126} , A_{127} }

[0087] bit-7-is-0 = {A_0 , A_3 , A_4 , A_7 , A_8, A_{11} , A_{12}, A_{15} ,A_{16}, A_{19}, A_{20}, A_{23} , A_{24}, A_{27} , A_{28}, A_{31} A_{32}, A_{35} , A_{36}, A_{39} , A_{40}, A_{43} , A_{44}, A_{47} , A_{48}, A_{51} , A_{52}, A_{55} , A_{56}, A_{59} , A_{60}, A_{63} , A_{64}, A_{67} , A_{68}, A_{71} , A_{72}, A_{75} , A_{76}, A_{79} , A_{80}, A_{83}, A_{84}, A_{87} , A_{88}, A_{91} , A_{92}, A_{95} A_{96}, A_{99} , A_{100}, A_{103}, A_{104}, A_{107}, A_{108}, A_{111} , A_{112}, A_{115}, A_{116}, A_{119}, A_{120}, A_{123}, A_{124}, A_{127}}

[0088] bit-7-is-1 = {A_1 , A_2 , A_5 , A_6, A_9 , A_{10}, A_{13} , A_{14}, A_{17} , A_{18}, A_{21}, A_{22}, A_{25} , A_{26}, A_{29} , A_{30}, A_{33} , A_{34}, A_{37} , A_{38}, A_{41} , A_{42}, A_{45} , A_{46}, A_{49} , A_{50}, A_{53} , A_{54}, A_{57} , A_{58}, A_{61} , A_{62}, A_{65}, A_{66}, A_{69} , A_{70}, A_{73} , A_{74}, A_{77} , A_{78}, A_{81} , A_{82}, A_{85} , A_{86}, A_{89} , A_{90}, A_{93} , A_{94}, A_{97}, A_{98}, A_{101}, A_{102}, A_{105}, A_{106}, A_{109}, A_{110}, A_{113}, A_{114}, A_{117}, A_{118}, A_{121}, A_{122}, A_{125} , A_{126} }

[0089] From each received symbol, R^k , the bit probabilities are computed as follows:

$$LLR(u_1^k) = \log\left(\frac{\sum_{A_i \in bit\text{-}1\text{-}is\text{-}1} \exp\left(-\frac{1}{2\sigma_N^2}\left\| R^k - A_i \right\|\right)}{\sum_{A_j \in bit\text{-}1\text{-}is\text{-}0} \exp\left(-\frac{1}{2\sigma_N^2}\left\| R^k - A_j \right\|\right)}\right) \quad (21)$$

$$LLR(u_2^k) = \log\left(\frac{\sum_{A_i \in bit\text{-}2\text{-}is\text{-}1} \exp\left(-\frac{1}{2\sigma_N^2}\left\| R^k - A_i \right\|\right)}{\sum_{A_j \in bit\text{-}2\text{-}is\text{-}0} \exp\left(-\frac{1}{2\sigma_N^2}\left\| R^k - A_j \right\|\right)}\right) \quad (22)$$

$$LLR(u_3^k)=\log\left(\frac{\sum_{A_i\in bit\text{-}3\text{-}is\text{-}1}\exp\left(-\frac{1}{2\sigma_N^2}\left\|R^k-A_i\right\|\right)}{\sum_{A_j\in bit\text{-}3\text{-}is\text{-}0}\exp\left(-\frac{1}{2\sigma_N^2}\left\|R^k-A_j\right\|\right)}\right) \quad (23)$$

$$LLR(u_4^k)=\log\left(\frac{\sum_{A_i\in bit\text{-}4\text{-}is\text{-}1}\exp\left(-\frac{1}{2\sigma_N^2}\left\|R^k-A_i\right\|\right)}{\sum_{A_j\in bit\text{-}4\text{-}is\text{-}0}\exp\left(-\frac{1}{2\sigma_N^2}\left\|R^k-A_j\right\|\right)}\right) \quad (24)$$

$$LLR(u_5^k)=\log\left(\frac{\sum_{A_i\in bit\text{-}5\text{-}is\text{-}1}\exp\left(-\frac{1}{2\sigma_N^2}\left\|R^k-A_i\right\|\right)}{\sum_{A_j\in bit\text{-}5\text{-}is\text{-}0}\exp\left(-\frac{1}{2\sigma_N^2}\left\|R^k-A_j\right\|\right)}\right) \quad (25)$$

$$LLR(u_6^k)=\log\left(\frac{\sum_{A_i\in bit\text{-}6\text{-}is\text{-}1}\exp\left(-\frac{1}{2\sigma_N^2}\left\|R^k-A_i\right\|\right)}{\sum_{A_j\in bit\text{-}6\text{-}is\text{-}0}\exp\left(-\frac{1}{2\sigma_N^2}\left\|R^k-A_j\right\|\right)}\right) \quad (26)$$

$$LLR(u_7^k)=\log\left(\frac{\sum_{A_i\in bit\text{-}7\text{-}is\text{-}1}\exp\left(-\frac{1}{2\sigma_N^2}\left\|R^k-A_i\right\|\right)}{\sum_{A_j\in bit\text{-}7\text{-}is\text{-}0}\exp\left(-\frac{1}{2\sigma_N^2}\left\|R^k-A_j\right\|\right)}\right) \quad (27)$$

[0090] An analogous computation effort is required for the bits of the Q dimension, the I^k being replaced with the Q^k demodulated value in order to evaluate $LLR(u_8^k)$, $LLR(u_9^k)$, $LLR(u_{10}^k)$, $LLR(u_{11}^k)$, $LLR(u_{12}^k)$, $LLR(u_{13}^k)$ and $LLR(u_{14}^k)$.

[0091] The bit error probabilities are provided to the outer decoder where they are used by the outer decoder to generate bit error information indicating the location of the erroneous bits and to selectively correct the erroneous bits.

[0092] As discussed above, conventional outer decoders comprise a first stage that determines bit error information from the output bits of the inner decoder themselves, and a second stage that corrects bits in accordance with the bit error information. In accordance with

the first preferred embodiment of the present invention, the first stage of the conventional outer decoder is replaced with a stage that generates a hard bit error decision for each bit using externally provided bit error probability information, such as by a thresholding procedure, and provides the bit error information to a second stage, such a conventional second stage, where bit errors are corrected in accordance with the bit error information. Those of ordinary skill in the art will be capable of modifying any of the conventional outer decoders of this type to accept externally generated bit error probability information and generated bit error information therefrom for use in the second stage of the decoder. Therefore no further detailed discussion of the outer decoder is provided here apart from the discussion in section 5 below.

[0093] These probabilities are used by the outer decoder to detect the location of the erroneous bits.

3.1.5.4 Simulation Results

[0094] Figure 5 shows the simulation results for 31200 information bits. A BER of 10^{-7} can be achieved after 8 iterations at $E_b/N_0 = 28.25$ dB.

4. IDFT use for ADSL systems

[0095] After the mapper, the signal is sent to the IDFT, shown as 5 in Figure 1 and to the channel, shown as 6 in Figure 1.

5. Use of the information by the Reed-Solomon outer decoder.

[0096] The received signal is sent to the DFT block, 7 in Figure 1, and to the inner decoder 7 in Figure 1.

[0097] The probabilities in equations (16), (17) and (18) for the case of 4 bit/s/Hz and the probabilities of equations (21), (22), (23), (24), (25), (26) and (27) for the case of 12 bit/s/Hz are used for the RS decoder, shown as 9 in Figure 1, in the following way:

[0098] The reliability of the received data is determined with the reliability of the MAP decoder. These data and associated bit error probabilities are carried through the deinterleaver placed between the inner decoder and the outer decoder. The Reed-Solomon uses as indication of error placement the worst of the bit error probabilities. Note that the MAP decoder may assign poor probabilities to all data associated with a frame .

[0099] While the first preferred embodiment utilizes turbo coding for the inner encoder and RS for the outer decoder, it will of course work with any soft-output inner encoder that provides bit error probabilities and outer encoders that utilize bit error probability information. This include turbo code base Maximum a Posteriori (MAP), Logarithmic MAP (LOGMAP), Maximum LAGMAP (MAXLOGMAP), soft-output Viterbi Algorithm (SOVA), Turbo Block Codes, as well as inner encoder using a single convolutional code as such trellis encoding of G.992.1 and G.992.2. It is recognized that the use of soft-output decoders on this non-turbo encoder will also give the same benefit. The significant point to recognize is the use of the inner soft-output decoder and that the outer decoder can take advantage of this information.

[00100] Accordingly, in accordance with the first preferred embodiment, there is a process for decoding a symbol stream with forward error correction to produce an information bit stream. This process is illustrated in Figure 6. A symbol stream is received 60 from a transmitter. The symbol stream is decoded 62 in an inner decoder using soft-output decoding to provide an output bit stream and associated bit error probabilities. The bit error probabilities and the output bit stream are provided 64 to an outer decoder, and the outer decoder produces 66 an information bit stream from the output bit stream using the bit error probabilities.

6. Second preferred embodiment using inner sum-product coding

[00101] In a second preferred embodiment, a sum-product algorithm inner encoder and decoder, such as LDPC coders, are used in a transmitter and receiver, respectively. The second preferred embodiment differs from the first preferred embodiment in that the sum-product inner decoder provides bit error information for its output bit stream, i.e. information indicating the position of each erroneous bit that requires correction by the outer decoder. The bit error information is provided to the outer decoder and used to select bits from the inner decoder output stream for correction in the outer decoder. This embodiment is preferred for its simplicity of implementation.

[00102] Accordingly, in accordance with the second preferred embodiment, there is a process in a transmitter for encoding a symbol stream with forward error correction from an information bit stream. As shown in Figure 7, an information bit stream is received 70 and is encoded in an outer encoder 72. The output of the outer encoder is encoded 74 in an inner

encoder using sum-product encoding. A symbol stream is then produced 76 by mapping an output bit stream of the inner encoder.

[00103] Further, in accordance with the second preferred embodiment, there is a process in a receiver for decoding a symbol stream with forward error correction to produce an information bit stream. As shown in Figure 8, a symbol stream is received 80 from a transmitter. The symbol stream is decoded 82 in an inner decoder using sum-product decoding to provide an output bit stream and bit error information for the output bit stream. The bit error information and the output bit stream are provided 86 to an outer decoder, and the outer decoder produces 88 an information bit stream from the bit error information and the output bit stream.

[00104] Further embodiments of the invention pertain to a transmitter or receiver that performs processing as described above. Typically such transmitter or receiver will comprise at least one processor and storage media coupled to the at least one processor and containing programming code for performing processing as described above.

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